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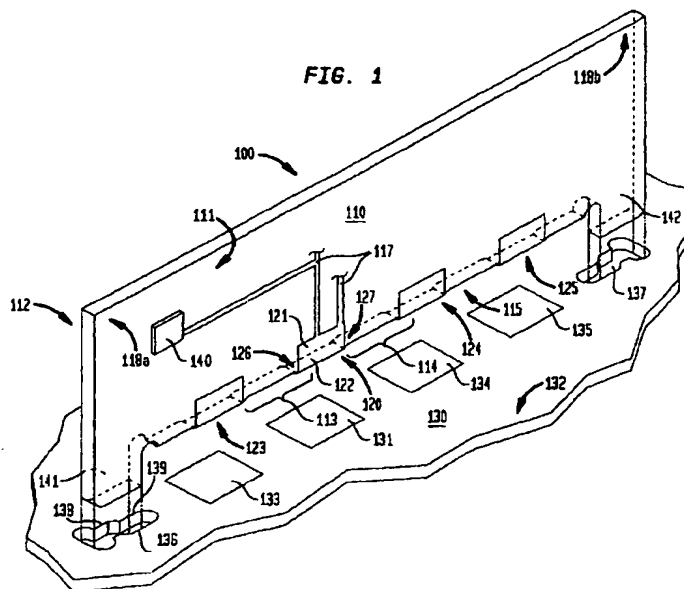
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(54) **Edge-mountable integrated circuit package and method of attaching the same to a printed wiring board**

(57) An edge-mountable integrated circuit (IC) package and methods of manufacturing and assembling the same onto a printed wiring board (PWB). In one embodiment, the package includes: (1) a substrate having a major surface and a substantially planar edge and (2) a conductive coating having a first region

located on a portion of the major surface and a second region located on a portion of the substantially planar edge, the second region being substantially planar to allow the second region to be reflow soldered to the adjoining printed wiring board PWB.



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## Description

### Technical Field Of The Invention

[0001] The present invention is directed, in general, to mounting techniques for electronic components and, more specifically, to an edge-mountable integrated circuit (IC) package and method of attaching the same to a printed wiring board (PWB).

### Background Of The Invention

[0002] The burgeoning electronics industry has been driven by consumer and commercial needs for more and more complex electronic assemblies in ever smaller spaces. With the conversion from vacuum tubes to integrated circuits, electronics transitioned from individual hand-wired components on a major chassis to printed wiring board (PWB) assemblies with integrated circuit subassemblies thereon. In the early days of electronics, virtually all of the electronic parts were interconnected by wires routed primarily on the underside of the chassis. As transistors, and then integrated circuits, came into widespread use, it became possible to group major electronic functions together on designated areas of the chassis. The chassis evolved to a "motherboard" when it became possible to move some functions to smaller PWBs or "daughterboards." The terms "motherboard" and "daughterboard" in this context are not limited to computer applications but include any electronic devices with PWBs that function in the general manner described.

[0003] PWB assemblies comprise a substantially flat, rectangular package having two parallel major surfaces and a number of minor surfaces, or edges, normal to the major surfaces. The major and minor surfaces are designated as such to indicate that a surface area of the major surface is greater than a surface area of the minor surface. Arbitrarily for the sake of this discussion, motherboards are considered to be mounted horizontally; however daughterboards, may mount horizontally or vertically. Of course, there are applications where the motherboard is vertical. Horizontal mounting places the major surfaces of the motherboard and daughterboard substantially parallel. Vertical mounting places the major surface of the daughterboard normal to the major surface of the motherboard. Vertical mounting also allows designers to package more electronics into less area of the motherboard, thereby reducing the overall footprint of the electronic devices. Therefore, some means of mechanically attaching and electrically interconnecting the PWB subassemblies/daughterboards to the motherboard is extremely important. Interconnecting the daughterboards for removable/replaceable functions, such as a modem, video card, disk drive controllers, etc., is usually accomplished by edge card connectors with friction fit contacts spaced 0.1" apart on center. Some daughterboard functional subassemblies,

however, are essential to the overall function of the electronic device and therefore require permanent connection to the motherboard. Traditionally, permanently installed, single in-line packages (SIPs) are electrically connected to the motherboard with either plug connectors or edge card connectors that can be reflow soldered to the motherboard. Alternatively, electrical connections between the daughterboard and the motherboard may be accomplished with wire when the boards are mechanically coupled without electrical interconnections. Of course, plug connectors, edge card connectors and wire connections add to the complexity and cost of the total assembly. Both of these techniques are expensive and have the additional disadvantage of unwanted inductance upon assembly.

[0004] Accordingly, what is needed in the art is an edge-mountable integrated circuit package and a method of attaching the package to a printed wiring board that minimizes both inductance, space and cost.

### Summary Of The Invention

[0005] To address the above-discussed deficiencies of the prior art, the present invention provides an edge-mountable integrated circuit (IC) package and methods of manufacturing and assembling the same onto a printed wiring board (PWB). In one embodiment, the package includes: (1) a substrate having a major surface and a substantially planar edge and (2) a conductive coating having a first region located on a portion of the major surface and a second region located on a portion of the substantially planar edge, the second region being substantially planar to allow the second region to be reflow soldered to the adjoining printed wiring board PWB.

[0006] The present invention therefore avoids the edge connectors and wire bonds of the prior art, allowing a substrate to be joined edge-on directly to a PWB. The present invention is effected by providing a conductive coating on the edge of the substrate, which then can be used in an otherwise conventional solder reflow process to join the substrate to the PWB.

[0007] In one embodiment of the present invention, the package further includes a second conductive coating having a first region located on a second portion of the major surface and a second region located on a second portion of the substantially planar edge, the second region of the second conductive coating being substantially planar to allow the second region to be concurrently reflow soldered to the adjoining PWB. Thus, a single edge can accommodate more than one region (terminal). In one embodiment to be illustrated and described, the second region extends over less than half a width of the substantially planar edge, allowing conductive coatings to be placed in tandem along the length of the substantially planar edge. Each conductive coating can be routed to its respective adjacent major surface, effectively doubling the number of terminals

that the package is allowed to have. Of course, tandem location need not be provided.

[0008] In one embodiment of the present invention, the substrate is composed of a resin-impregnated glass fiber. However, other conventional and later-discovered substrate materials that are capable of accommodating a conductive coating are within the broad scope of the present invention.

[0009] In one embodiment of the present invention, the first region comprises a conductive trace. Thus, the coating may be coupled to, or form a part of, a conventional surface or inter-layer trace for conducting current along or under the major surface.

[0010] In one embodiment of the present invention, the package further includes first and second extensions projecting from the substantially planar edge and adapted to engage corresponding first and second apertures in the PWB. In a more specific embodiment of the present invention, the package further includes the PWB and wherein the first and second apertures have an offset periphery to impress a bending moment on the substrate when the first and second extensions are engaged in the corresponding apertures. In an embodiment to be illustrated and described, the apertures may be formed by a rotating tool having a diameter exceeding the thickness of the substrate. The apertures can be employed to place the substrate in a bind, frictionally securing the substrate to the PWB pending reflow soldering.

[0011] In one embodiment of the present invention, the substantially planar edge contains first and second notches. The first notch is located proximate a first edge of the conductive coating. The second notch is located proximate a second edge of the conductive coating. The notches ensure that the substantially planar edge having the conductive coating stands out such that it can contact the PWB. This is advantageous if the PWB is not absolutely planar.

[0012] The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

#### **Brief Description Of The Drawings**

[0013] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompa-

nying drawings, in which:

FIGURE 1 illustrates an isometric view of one embodiment of an edge-mountable integrated circuit package constructed according to the principles of the present invention;

FIGURE 2 illustrates two alternative embodiments of the conductive coating 120 of FIGURE 1;

FIGURE 3 illustrates an exploded view of the edge-mountable integrated circuit package of FIGURE 2 during manufacture; and

FIGURE 4 illustrates an enlarged inverted view of the second embodiment of FIGURE 2.

#### **Detailed Description**

[0014] Referring initially to FIGURE 1, illustrated is an isometric view of one embodiment of an edge-mountable integrated circuit package constructed according to the principles of the present invention. An edge-mountable integrated circuit package, generally designated 100, comprises a substrate 110 and a conductive coating 120. In one advantageous embodiment, the substrate 110 may be constructed of a resin-impregnated glass fiber; however, one who is skilled in the art will recognize that other similar materials may also be used. The substrate 110 has two, essentially parallel, major surfaces 111, 112 and a substantially planar edge 115 normal to the major surfaces 111, 112. The conductive coating 120 may include a first major surface component or first region 121 located on a portion of the major surface 111, and an edge component or second region 122 located on a portion of the edge 115. The first region 121 and the second region 122 are contiguous so as to be electrically conductive. Connected to the first region 121 are conductive traces 117 that provide an electrical pathway for current from the conductive coating 120 to electronic components 140 mounted on the substrate 110. One who is skilled in the art is familiar with the conventional processes used to form conductive coatings 120, 117 on the substrate 110. The second region 122 is shown proximate a conductive region 131 on a surface 132 of a motherboard 130. Of course, multiple conductive coatings 123, 124, 125 may be formed on the substrate 110 as required for a particular application to mate with corresponding conductive regions 133, 134, 135.

[0015] In one embodiment, the edge-mountable integrated circuit package 100 may further comprise first and second notches 113, 114 located in the substantially planar edge 115. The first notch 113 is located proximate a first edge 126 of the conductive coating 120 and the second notch is located proximate a second edge 127 of the conductive coating 120. Contact between the second region 122 and the conductive

region 131 is assured by notching the substantially planar edge 115 as shown.

[0016] In another embodiment, the edge-mountable integrated circuit package 100 may further comprise first and second extensions 141, 142 projecting from the planar edge 115. Of course, any number of extensions may be provided to advantage. The first and second extensions 141, 142 are adapted to engage corresponding first and second apertures 136, 137 in the motherboard 130. In one advantageous embodiment, the first and second apertures 136, 137 have an offset periphery 138, 139 that impresses a bending moment 118a, 118b on the substrate 110 when the first and second extensions 141, 142 are inserted into the corresponding apertures 136, 137. This bending moment 118a, 118b holds the integrated circuit package 100 in proper alignment with the motherboard 130 during reflow soldering of the second region 122 to the conductive region 131.

[0017] To effect an electrical connection, the edge-mountable integrated circuit package 100 is mechanically installed on the motherboard 130 with the first and second extensions 141, 142 engaging the first and second apertures 136, 137. The edge-mountable integrated circuit package 100 and the motherboard 130 are then reflow soldered in a conventional manner forming an electrical connection between the second region 122 and the conductive region 131. One who is skilled in the art is familiar with reflow soldering.

[0018] Referring now to FIGURE 2, illustrated are two alternative embodiments of the conductive coating 120 of FIGURE 1. In this embodiment, an edge-mountable integrated circuit package 200 comprises a substrate 210, a first conductive coating 220 and a second conductive coating 230. The first conductive coating 220 has first and second conductive surface components 221, 222 and a common conductive edge component 223. Conductive surface component 221 is located on a portion of a first major surface 211, while second conductive surface component 222 is located on a portion of a second major surface 212. The first and second conductive surface components 221, 222 share the common conductive edge component 223 as shown. In this embodiment, electrical traces (not shown) similar to the electrical traces 117 of FIGURE 1 may be formed on both the first and second major surfaces 211, 212 as required. The common conductive edge component 223 is shown proximate its mating conductive region 260.

[0019] In an alternative embodiment, the second conductive coating 230 similarly comprises first and second conductive surface components 231, 232 on the first major surface 211 and second major surface 212, respectively. However, in this embodiment, two edge components 233, 234 have been formed. Each edge component 233, 234 extends over less than half a width of an edge 215 of the substrate 210. Thus, edge components 233, 234 may be coupled simultaneously through

reflow soldering with corresponding conductive regions 235, 236, respectively, on a motherboard 240.

[0020] In another embodiment, alternative apertures 238, 239 may be oblong in shape and cut to a width 244 that is slightly less than a thickness 214 of the substrate 210. Thus, a friction fit between the alternative apertures 238, 239 and first and second extensions 241, 242 holds the package 200 securely to the motherboard 240 during reflow soldering.

[0021] In an alternative embodiment, the substrate 210 may be manufactured to an overall length 207 such that the overall length 207 and a distance 243 between the first and second apertures 238, 239 will cooperate to create a slight compressive force 250 on the integrated circuit package 200 when the package 200 is installed in the motherboard 240. This compressive force 250 holds the integrated circuit package 200 in proper alignment with the motherboard 240, and the common conductive edge component 223 in contact with conductive region 260 and edge components 233, 234 in contact with corresponding conductive regions 235, 236 during reflow soldering.

[0022] Referring now to FIGURE 3, illustrated is an exploded view of the edge-mountable integrated circuit package of FIGURE 2 during manufacture. The common conductive edge component 223 may be formed on the substrate 210 by forming an aperture 310 through the substrate 210. The first and second conductive surface components 221, 222 and the common conductive edge component 223 are formed simultaneously by plating. Excess material 320 is then cut from the edge-mountable integrated circuit package 200 along cut line 325 forming the substantially planar edge 215 and first and second notches 213, 214.

[0023] Referring now to FIGURE 4, illustrated is an enlarged inverted view of the second embodiment of FIGURE 2. Shown is the second conductive coating 230 comprising the first and second conductive surface components 231, 232 and the two edge components 233, 234. The two edge components 233, 234 are separated by a kerf 410 in the edge 215 of the substrate 210. Also shown is an edge 415 of the substrate 210 having first and second notches 416, 417 with arcuate portions 420, 430 that allow the edge components 233, 234 to extend slightly so as to assure a positive contact with the conductive regions 235, 236 of FIGURE 2. The shape of portions 420, 430, may also be a decline, or any other shape that is readily manufacturable and suitable for providing clearance between the substrate edge 415 and the surface 132 of the motherboard 130.

[0024] From the above, it is apparent that the present invention provides an edge-mountable IC package and methods of manufacturing and assembling the same onto a PWB. In one embodiment, the package includes: (1) a substrate having a major surface and a substantially planar edge and (2) a conductive coating having a first region located on a portion of the major surface and a second region located on a portion of the

substantially planar edge, the second region being substantially planar to allow the second region to be reflow soldered to the adjoining printed wiring board PWB.

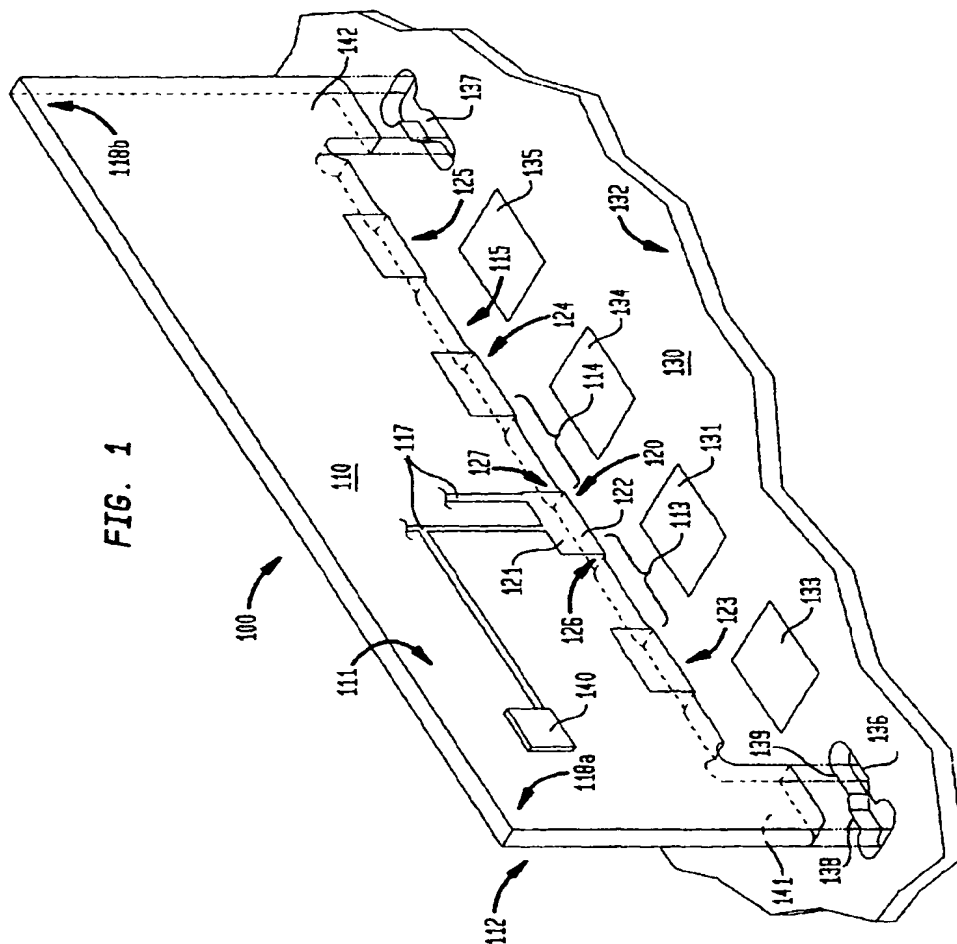
[0025] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

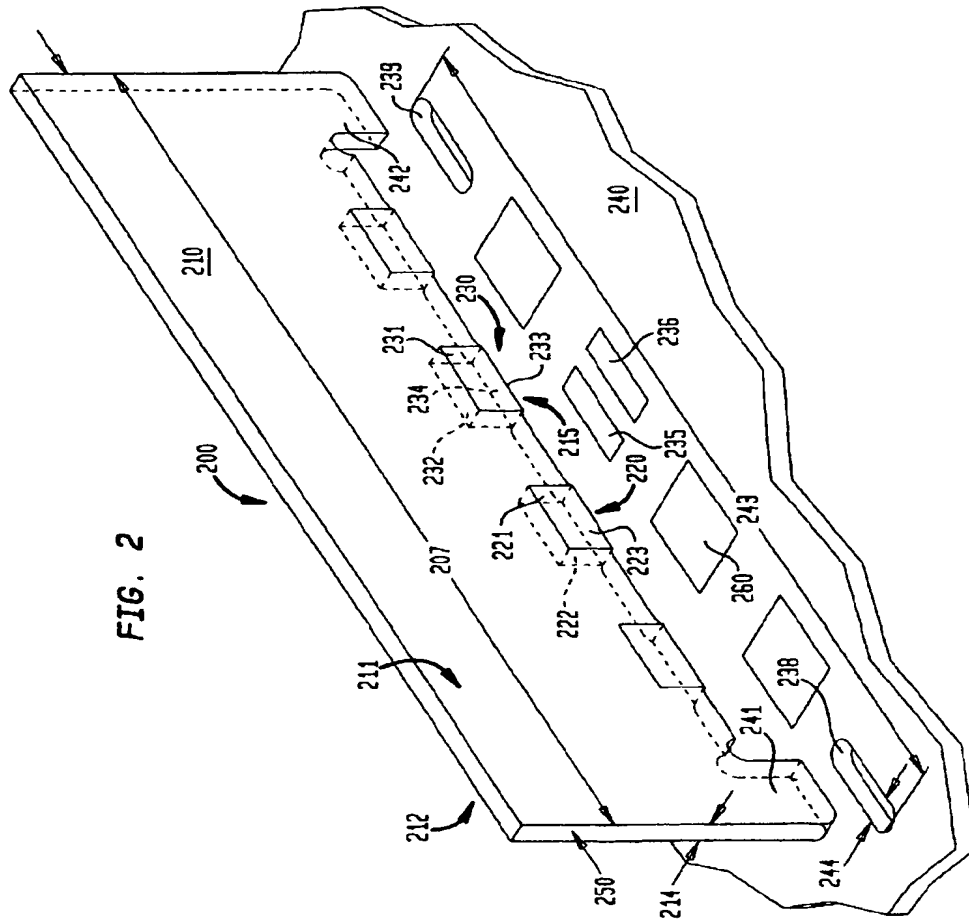
#### Claims

1. An edge-mountable integrated circuit (IC) package, comprising:
  - a substrate having a major surface and a substantially planar edge; and
  - a conductive coating having a first region located on a portion of said major surface and a second region located on a portion of said substantially planar edge, said second region being substantially planar to allow said second region to be reflow soldered to an adjoining printed wiring board (PWB).
2. The package as recited in Claim 1 further comprising a second conductive coating having a first region located on a second portion of said major surface and a second region located on a second portion of said substantially planar edge, said second region of said second conductive coating being substantially planar to allow said second region of said second conductive coating to be concurrently reflow soldered to said adjoining PWB.
3. The package as recited in Claim 1 wherein said second region extends over less than half a width of said substantially planar edge.
4. The package as recited in Claim 1 wherein said substrate is composed of a resin-impregnated glass fiber.
5. The package as recited in Claim 1 wherein said first region comprises a conductive trace.
6. The package as recited in Claim 1 further comprising first and second extensions projecting from said substantially planar edge and adapted to engage corresponding first and second apertures in said PWB.
7. The package as recited in Claim 6 further comprising said PWB and wherein said first and second apertures have an offset periphery to impress a bending moment on said substrate when said first and second extensions are engaged in said corresponding apertures.
8. The package as recited in Claim 1 wherein said substantially planar edge contains first and second notches, said first notch located proximate a first edge of said conductive coating and said second notch located proximate a second edge of said conductive coating.
9. A method of manufacturing an edge-mountable integrated circuit (IC) package, comprising:
  - providing a substrate having a major surface and a substantially planar edge; and
  - creating a conductive coating having a first region located on a portion of said major surface and a second region located on a portion of said substantially planar edge, said second region being substantially planar to allow said second region to be reflow soldered to an adjoining printed wiring board (PWB).
10. The method as recited in Claim 9 further comprising creating a second conductive coating having a first region located on a second portion of said major surface and a second region located on a second portion of said substantially planar edge, said second region of said second conductive coating being substantially planar to allow said second region of said second conductive coating to be concurrently reflow soldered to said adjoining PWB.
11. The method as recited in Claim 9 wherein said second region extends over less than half a width of said substantially planar edge.
12. The method as recited in Claim 9 wherein said substrate is composed of a resin-impregnated glass fiber.
13. The method as recited in Claim 9 wherein said creating comprises forming an aperture in said substrate, coating an interior surface of said aperture with said conductive coating and cutting said substrate to cause a portion of said aperture to form said substantially planar edge.
14. The method as recited in Claim 9 further comprising forming first and second extensions projecting from said substantially planar edge and adapted to engage corresponding first and second apertures in said PWB.
15. The method as recited in Claim 14 further comprising coupling said PWB and said package and wherein said first and second apertures have an offset periphery to impress a bending moment on said substrate when said first and second extensions are engaged in said corresponding apertures.

16. The method as recited in Claim 9 further comprising forming first and second notches in said substantially planar edge, said first notch located proximate a first edge of said conductive coating and said second notch located proximate a second edge of said conductive coating. 5
17. A method of mounting an edge-mountable integrated circuit (IC) package to a printed wiring board, comprising: 10
- providing a substrate having a major surface and a substantially planar edge and a conductive coating having a first region located on a portion of said major surface and a second region located on a portion of said substantially planar edge; 15
- placing said second region directly in contact with a bonding pad on said PWB; and 20
- reflow soldering said second region to said bonding pad.
18. The method as recited in Claim 17 wherein said package further has a second conductive coating having a first region located on a second portion of said major surface and a second region located on a second portion of said substantially planar edge, said method further comprising concurrently reflow soldering said second region of said second conductive coating to said adjoining PWB. 25 30
19. The method as recited in Claim 17 wherein said second region extends over less than half a width of said substantially planar edge. 35
20. The method as recited in Claim 17 wherein said substrate is composed of a resin-impregnated glass fiber. 40
21. The method as recited in Claim 17 wherein said first region comprises a conductive trace.
22. The method as recited in Claim 17 further comprising engaging first and second extensions projecting from said substantially planar edge into corresponding first and second apertures in said PWB. 45
23. The method as recited in Claim 22 further comprising impressing a bending moment on said substrate when said first and second extensions are engaged in said corresponding apertures. 50

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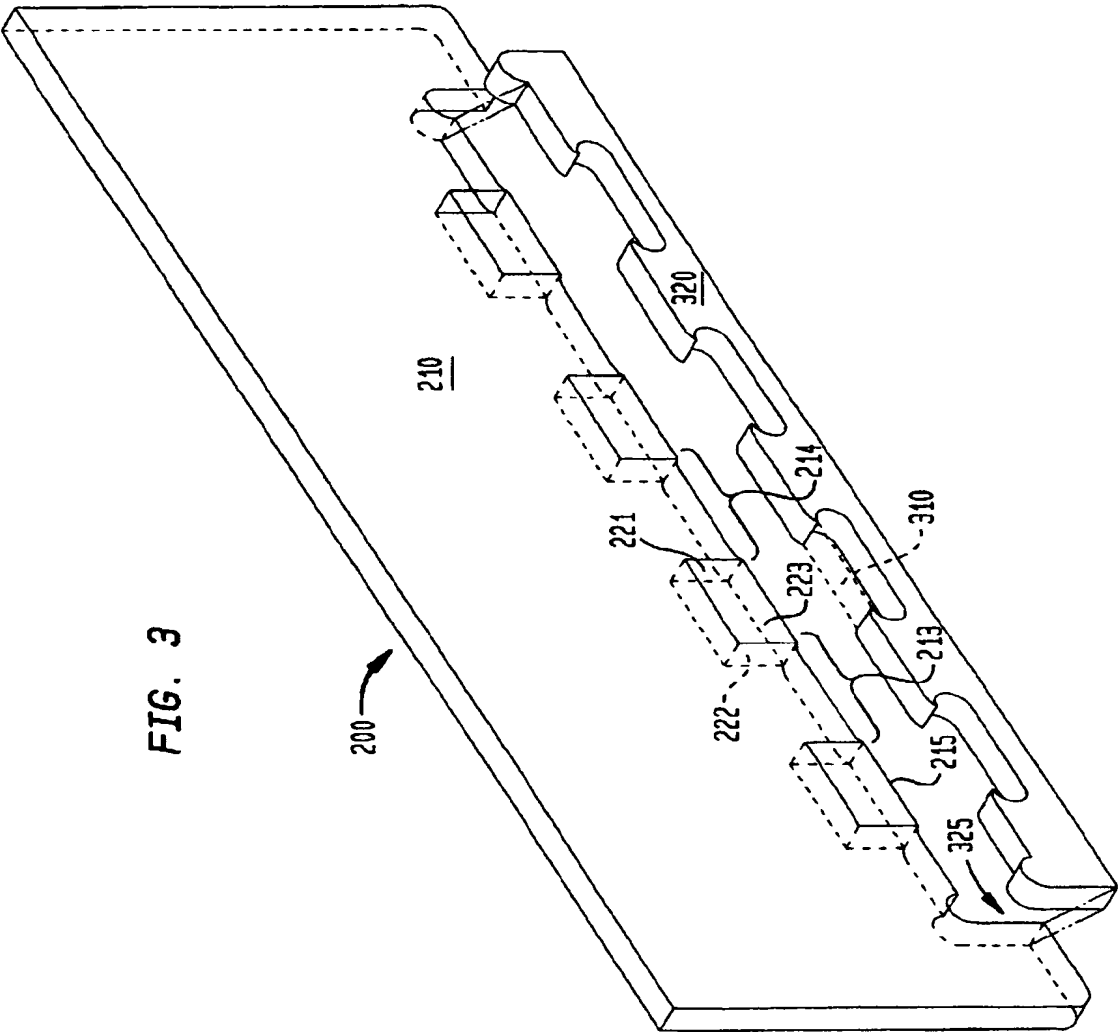
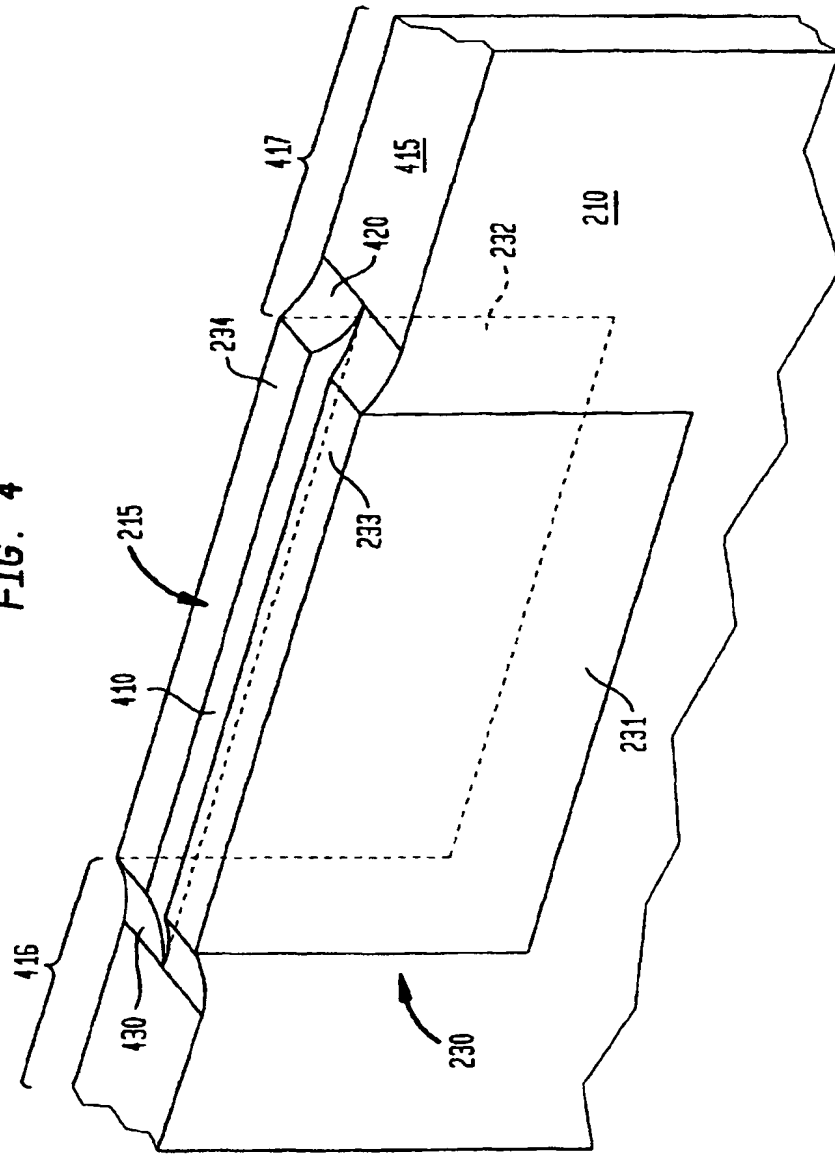
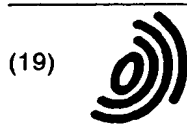


FIG. 4





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(30) Priority: **11.03.1999 US 266531**

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(54) **Edge-mountable integrated circuit package and method of attaching the same to a printed wiring board**

(57) An edge-mountable integrated circuit (IC) package (100) and methods of manufacturing and assembling the same onto a printed wiring board (PWB) (130). In one embodiment, the package (100) includes: 1) a substrate (110) having a major surface (111) and a substantially planar edge (115) and 2) a conductive

coating (120) having a first region (121) located on a portion of the major surface (111) and a second region (122) located on a portion of the substantially planar edge (115), the second region (122) being substantially planar to allow the second region (122) to be reflow soldered to the adjoining printed wiring board PWB (130).

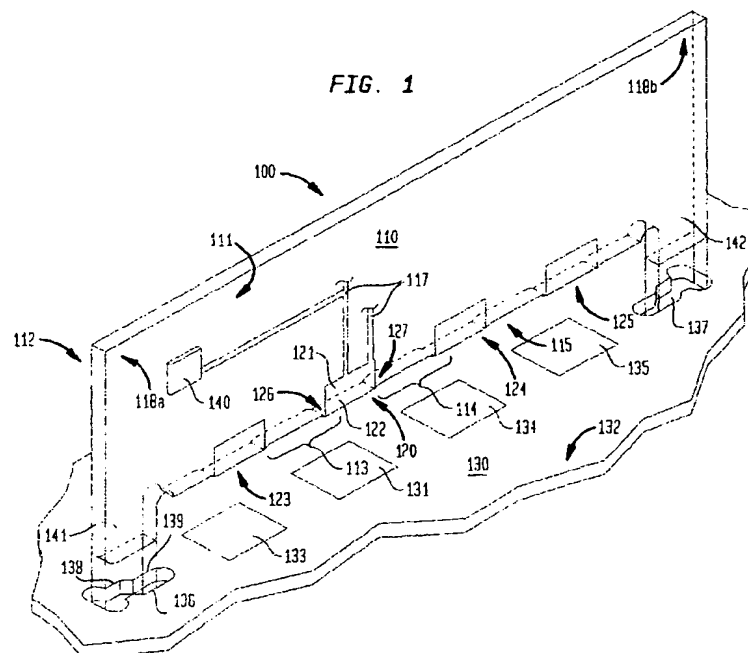


FIG. 1



European Patent  
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# EUROPEAN SEARCH REPORT

Application Number  
EP 00 30 1558

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 621 619 A (SEFFERNICK ET AL.) 15 April 1997 (1997-04-15)	1-3, 5, 6, 8-11, 14, 16-19, 21, 22	H05K3/36 H05K3/40 H01L23/498
Y	* the whole document *	13	
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 05, 31 May 1996 (1996-05-31) -& JP 08 023163 A (TANAKA KIKINZOKU KOGYO KK), 23 January 1996 (1996-01-23) * abstract; figures *	1, 2, 6, 9, 10, 14, 17, 18, 22	
Y		13	
X	GB 2 137 805 A (BRACEY) 10 October 1984 (1984-10-10)	1, 2, 4, 5, 9, 10, 12, 17, 18, 20, 21	
	* page 1, line 2 - line 8 * * page 1, line 97 - line 100 * * page 3, line 84 - line 90; figure 28 *		TECHNICAL FIELDS SEARCHED (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 144 (E-1521), 10 March 1994 (1994-03-10) -& JP 05 327161 A (FUJITSU LTD), 10 December 1993 (1993-12-10) * abstract; figures *	1, 2, 5, 6, 9, 10, 14, 17, 18, 21, 22	H05K
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 444 (E-1265), 16 September 1992 (1992-09-16) -& JP 04 155991 A (TAIYO YUDEN CO LTD), 28 May 1992 (1992-05-28) * abstract; figures *	1, 2, 5, 9, 10, 17, 18	
A		6, 14, 22	
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	-/--		
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		11 December 2002	Mes, L
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons & : member of the same patent family, corresponding document	

EPQ FORM 1503 03 82 (F04C01)



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Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 00 30 1558

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	<p>EP 0 040 379 A (GENERAL ELECTRIC COMPANY) 25 November 1981 (1981-11-25)</p> <p>* page 5, line 5 - line 9 * * page 6, line 4 - line 14 * * page 7, line 12 - page 8, line 5 * * figures *</p> <p>-----</p>	1,2,4, 8-10,12, 16-18,20	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
The present search report has been drawn up for all claims			
Place of search <b>THE HAGUE</b>		Date of completion of the search <b>11 December 2002</b>	Examiner <b>Mes, L</b>
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>I : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application F : document cited for other reasons &amp; : member of the same patent family, corresponding document</p>			

EPO FORM 1503 (02.92) (P04001)

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on  
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11-12-2002

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5621619	A	15-04-1997	DE 4135007 A1	14-05-1992
			FR 2673063 A1	21-08-1992
			GB 2249746 A ,B	20-05-1992
			IT 1250024 B	30-03-1995
			JP 3342706 B2	11-11-2002
			JP 4264701 A	21-09-1992
JP 08023163	A	23-01-1996	NONE	
GB 2137805	A	10-10-1984	GB 2155096 A ,B	18-09-1985
JP 05327161	A	10-12-1993	NONE	
JP 04155991	A	28-05-1992	NONE	
EP 0040379	A	25-11-1981	EP 0040379 A1	25-11-1981
			JP 57017193 A	28-01-1982

EPO FORM 10459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82